

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHIVALING S. MAHANT-SHETTI
and VIVEK G. PAWAR

Appeal No. 96-3667
Application No. 08/176,867¹

ON BRIEF

Before URYNOWICZ, JERRY SMITH and RUGGIERO, Administrative
Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 1-6,
8, 9, 11 and 14-16.

¹ Application for patent filed December 30, 1993.

The invention pertains to a method and apparatus for determining a Hamming distance between two multi-bit digital words. Claim 1 is illustrative and reads as follows:

1. A device for determining a Hamming distance between two multi-bit digital words, comprising:

circuitry for determining nonmatching bit positions of the two multi-bit digital words;

circuitry for generating a current signal for each nonmatching bit position, said current signal having a selected fixed current level, and a summed current signal from said generated current signals, said summed current signal having a current level representing the sum of said current signals;

circuitry for successively comparing said summed current signal with a plurality of reference current signals, said reference current signals being selected fixed current levels; and

circuitry for converting results of said comparing circuitry into a digital representation of the Hamming distance between the two multi-bit digital words.

The references relied upon by the examiner as evidence of obviousness are:

Clapper	2,885,149	May 05, 1959
Conway	3,656,109	Apr. 11, 1972
Basehore et al. (Basehore)	5,218,562	Jun. 08, 1993

Selviah et al. (Selviah), "Extension of the Hamming Neural Network to a Multilayer Architecture for Optical Implementation", IEEE, 1989, pages 280-283.

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Claims 1, 4 and 5 stand rejected under 35 U.S.C. § 103 as unpatentable over Basehore in view of Clapper.

Claims 2 and 3 stand rejected under 35 U.S.C. § 103 as unpatentable over Basehore in view of Clapper and Conway.

Claims 6, 8, 9 and 11 stand rejected under 35 U.S.C. § 103 as unpatentable over Basehore in view of Clapper and Selviah.

Claims 14-16 stand rejected under 35 U.S.C. § 103 as unpatentable over Basehore in view of Clapper, Conway and Selviah.

The respective positions of the examiner and the appellants with regard to the propriety of these rejections are set forth in the examiner's final rejection and answer (Paper Nos. 5 and 9, respectively) and the appellants' brief (Paper No. 8).

Appellants' Invention

The invention determines the number of bits differing between two multibit words (Hamming distance) by converting bit differences to currents which are summed. The sum is compared to reference currents to generate outputs. Figure 2 illustrates apparatus wherein bit differences from bit comparator 12 turn on

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transistors 30-32 which have their summed currents mirrored via current mirrors 34-36, 34-42 and 34-54 into current comparators 18, 20 and 22. Current comparator 18 compares the summed current with 4 times the current I generated by a single bit difference. Current comparator 20 compares the summed current with 2 or 6 times I, and current comparator 22 compares the summed current with 1, 3, 5 or 7 times I. Current comparator 20 uses the output of current comparator 18 to select comparison with either 2 or 6 times I, and current comparator 22 uses the outputs of both current comparators 18 and 20 to select comparison with one of 1, 3, 5 or 7 times I. Thus, the three current comparators can detect 8 levels of summed current and, consequently, Hamming distances from 0 to 7.

Opinion

Appellants have not specifically argued the patentability of any claim other than claim 1. Accordingly, claims 2-6, 8, 9, 11 and 14-16 stand or fall with claim 1. In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987).

Appellants admit that Clapper shows a full adder using bipolar transistors but argue that neither Clapper nor Basehore,

nor any of the other references, shows or suggests any current comparisons as required by the third element of claim 1. With respect to Figure 1 of Clapper, it is urged that three inputs A, B and C drive emitter followers 16, 26 and 30 which, in turn, bias current sources 32, 36 and 39 having common collectors. The collector currents generated in response to the A, B and C inputs are coupled to a -15 volt reference through resistor 34, and are thereby converted to a voltage at node E which is proportional to the sum of the three collector currents. This voltage level is then compared to three thresholded outputs which have different threshold voltages, and thereby produce the sum and carry voltage signals. Figure 3 shows the four possible voltage levels on node E and the resultant sum and carry outputs. This is a voltage level operation and only voltage comparisons are performed in the outputs. Because there is no teaching of current comparison, as in claim 1 and all of the other claims on appeal, it is urged that the claims are patentable over the prior art.

The examiner admits that Basehore does not disclose current adders and comparators, and that instead Basehore utilizes digital computation. It is urged that Clapper discloses an adder which uses current generators and transistors to represent a

predetermined increment of current to flow and represent a specific signal, and that it would have been obvious to compare current signals at selected fixed current levels in Basehore's system because this would have allowed for the accurate representation of signals with little power loss. The examiner states in the answer at page 4,

However, it is well known in the art that voltage signals are more accurate than current signals and that current signals have less power dissipation than voltage signals. The examiner asserts that it would have been obvious to one of ordinary skill to compare signals in a current or voltage, the difference being the use of a resistor, because this would allow optimal comparison of signals according to the system requirements. If one wanted less power dissipation, the employment of current comparisons would be optimal.

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejections should not be sustained. Each of the claims requires the comparison of current signals, and it is considered that the examiner has not established that it would have been obvious to modify the combined teachings of Basehore and Clapper, which references are common to all of the rejections, to compare current signals as opposed to voltage signals so as to

incur less power dissipation². The examiner has drawn attention to no evidence which teaches that power dissipation was a problem in the prior art because voltage signals were compared. There is simply no evidence establishing facts which would have motivated one of ordinary skill in the art to modify the prior art as suggested by the examiner. The mere fact that the prior art may have been modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d

²With respect to this issue of comparing current signals, the prior art to Conway and Selviah et al. are not relied on by the examiner.

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1260, 1266, 23 USPQ2d 1780, 1782-1783 (Fed. Cir. 1992).

REVERSED

STANLEY M. URYNOWICZ, JR.)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JERRY SMITH)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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JOSEPH F. RUGGIERO)	
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SMU/gjh

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REVERSED

Prepared: November 10, 1999